

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Lysander Lim

Serial No. N/A

Filed: Herewith

For: FREQUENCY SYNTHESIZER FOR A
WIRELESS COMMUNICATION
SYSTEM

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Examiner: N/A

Group Art Unit: N/A

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The cited patents are listed in numerical order and are not in any order based on their pertinence.

Pursuant to the waiver of the requirement under 37 CFR 1.98 (a)(2)(i) as stated in a Pre-OG Notice dated July 11, 2003, copies of only the foreign patent documents and non-patent literature listed on the enclosed modified Form PTO-1449 are attached.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,



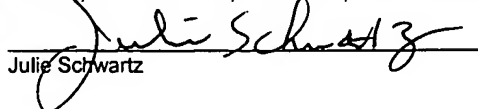
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EXPRESS MAIL NO.: EV396290821US

DATE OF DEPOSIT: 03/31/2004

This paper and fee are being deposited with the U. S. Postal Service Express Mail Post Office to Addressee service under 37 CFR § 1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450


Julie Schwartz

In place of PTO-1449 Form		U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	N/A
				Filing Date	Herewith
				Applicant(s)	Lysander Lim
				Art Unit	N/A
				Examiner Name	N/A
SHEET	1	OF	3	Attorney Docket Number	23119.8

U. S. PATENT DOCUMENTS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	1	6,137,372	10-24-2000	Welland
	2	6,147,567	11-14-2000	Welland et al.
	3	6,150,891	11-21-2000	Welland et al.
	4	6,167,245	12-26-2000	Welland et al.
	5	6,226,506	05-01-2001	Welland et al.
	6	6,233,441	05-15-2001	Welland
	7	6,304,146	10-16-2001	Welland
	8	6,308,055	10-23-2001	Welland et al.
	9	6,311,050	10-30-2001	Welland et al.
	10	6,317,006	11-13-2001	Welland et al.
	11	6,323,735	11-27-2001	Welland et al.
	12	6,327,463	12-04-2001	Welland
	13	2002/0008585	01-24-2002	Welland
	14	2002/0009984	01-24-2002	Welland et al.
	15	2002/0033714	03-21-2002	Perrott
	16	2002/0034932	03-21-2002	Welland
	17	2002/0041216	04-11-2002	Welland et al.
	18	6,388,536	05-14-2002	Welland
	19	2002/0089356	07-11-2002	Perrott et al.
	20	6,483,390	11-19-2002	Welland
	21	6,549,764	04-15-2003	Welland
	22	6,549,765	04-15-2003	Welland et al.
	23	6,574,288	06-03-2003	Welland et al.
	24	6,580,376	06-17-2003	Perrott
	25	2003/0119467	06-26-2003	Welland et al.
	26	6,590,426	07-08-2003	Perrott
	27	6,630,868	10-07-2003	Perrott et al.

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code - Number - Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N

OTHER PRIOR ART		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume- issue number(s), publisher, city/country where published
	28	ABRAMOVITCH, Danny, "Phase-Locked Loops: A Control Centric Tutorial", (May 8, 2002), pp.1-50, Agilent Laboratories, Communications and Optics Research Lab.
	29	ALFKE, Peter, "Frequency/Phase Comparator for Phase-Locked Loops", Application Note, (December 2, 1996), pp.1-2, Version 1.1, Xilinx, Inc.

Examiner Signature		Date Considered	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	30	ANALOG DEVICES, INC., "A Technical Tutorial on Digital Signal Synthesis", (1999), pp. 1-122.
	31	ANADIGM, INC., "Understanding Switched Capacitor Basics", Anadigmvortex Technical Training, (November 2002), pp. 1-25.
	32	CRANINCKX, et al., "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer", (1998), pp. 1-10, Institute of Electrical and Electronics Engineers, Inc.
	33	CURTIN, et al., "Phase-Locked Loops for High-Frequency Receivers and Transmitters – Part 1", (1999), pp. 1-4, 33-3, Analog Devices, Inc.
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	35	CURTIN, et al., "Phase-Locked Loops for High-Frequency Receivers and Transmitters – Part 3", (1999), pp. 1-5, 33-7, Analog Devices, Inc.
	36	DE MUER, et al., "A 1.8 GHz CMOS $\Delta\Sigma$ Fractional-N Synthesizer", (2001), Department of Electrical Engineering (ESAT) – MICAS, Katholieke Universiteit Leuven.
	37	DE MUER, Bram, "Monolithic CMOS Fractional- N Synthesizer", (November 2002), pp. 142-144, Katholieke Universiteit Leuven.
	38	FORSTER, Edward, "The Phase/Frequency Comparator Simplified", (1997).
	39	HERZEL, et al., "An Integrated CMOS RF Synthesizer for 802.11a Wireless LAN", IEEE Journal of Solid-State Circuits, (October 2003), pp. 1767-1770, Vol. 38, No. 10, Institute of Electrical and Electronics Engineers, Inc.
	40	JAMES, Norman, "CycleSim: A Phase-Locked Loop Simulator", (November 1999), Embedded Systems.
	41	KOO, et al., "A Fully-Integrated CMOS Frequency Synthesizer with Charge-Averaging Charge Pump and Dual-Path Loop Filter for PCS- and Cellular-CDMA Wireless Systems", IEEE Journal of Solid-State Circuits, (May 2002), pp. 536-542, Volume: 37, No. 5, (Abstract only), Institute of Electrical and Electronics Engineers, Inc.
	42	LACANETTE, Kerry, "A Basic Introduction to Filters – Active, Passive, and Switched-Capacitor", National Semiconductor Application Note, (April 1991), pp. 1-22, National Semiconductor Corporation.
	43	MARTIN, Ken, "Phase-Locked Loops", (2004), pp.1-55, Department of Electrical and Computer Engineering, University of Toronto.
	44	LeCROY CORPORATION, "Phase Locked Loop Basics: An Introduction to Phase Locked Loops", (2004), LeCroy Applications Brief No. L.A.B. 1007.
	45	MAXIM INTEGRATED PRODUCTS, INC., Charge Pumps Shine in Portable Designs", Application Note 669, (March 15, 2001), pp. 1-15.
	46	MINI-CIRCUITS, "Phase Locked Loop Fundamentals", (1999).
	47	NASH, Garth, "Phase-Locked Loop Design Fundamentals", Application Note, (1994), pp.1-12, Motorola, Inc.

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SHEET	3	OF	3	Attorney Docket Number	23119.8

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Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume- issue number(s), publisher, city/country where published
	48	PHILIPS SEMICONDUCTOR, "An Overview of the Phase-Locked Loop (PLL)", Application Note AN177, (December 1988), pp.1-6.
	49	SINHA, Saurabh "Design of an Integrated CMOS PLL Frequency Synthesizer", (2002) Signal Processing Systems, Department of Electrical Engineering, Technische Universiteit Eindhoven.
	50	UNIVERSITY OF SEOUL, "Discrete-Time Filter (Switched-Capacitor Filter)", (1996- 2000), IC Lab, Institute of Electrical and Electronics Engineers, Inc.

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